IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: **Davis, et al.**	§	Serial No.: **10/805,136**
Filed: **March 19, 2004**	§	Confirmation No.: **8916**
Docket No.: **APPM/8381/ETCH/SILICON**	§	Group Art Unit: **1765**
For: **Method For Controlling A Process For Fabricating Integrated Devices**	§	Examiner: **Angadi, Maki A.**

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REPLY BRIEF

In response to the Examiner's Answer dated on March 12, 2008, the Appellants hereby submit this Reply Brief to the Board of Patent Appeals and Interferences. The Appellants believe that no fees are due in connection with this submission. However, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees, including extension of time fees, required to make this response timely and acceptable to the Office.

REAL PARTY IN INTEREST

The real party in interest is Applied Materials, Inc., located in Santa Clara, California.

RELATED APPEALS AND INTERFERENCES

The Appellants know of no related appeal and/or interference that may directly affect or be directly effected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1, 3-21 and 36-53 are pending in the application. Claims 1, 3-21 and 36-53 stand rejected as discussed below. Claims 2 and 28-35 have been cancelled. Claims 22-27 have been withdrawn. The rejections of claims 1, 3-21 and 36-53 as set forth in the Final Office Action dated May 30, 2007 are appealed. The pending appealed claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

No amendments to the claims were submitted in this application subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides methods for controlling a process for fabricating integrated devices on a substrate. The claimed limitations may be understood with reference to Figures 1 and 2A-C and as annotated below.

In the embodiment of independent claim 1, a method of controlling a process of fabricating integrated devices on a substrate includes: measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate (*see*, *e.g.*, ¶[0023], [0035]; Figs. 1, 2A-B (step 204, 211)); adjusting a process recipe of an etch process for etching the substrate and a process recipe of at least one post-etch process using the results of measuring the dimensions on the structures (*see*, *e.g.*, ¶[0036]-[0037]; Fig. 2A-B (step 206, 207)); and executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch

process, and at least one post-etch process while forming the at least one structure (*see*, *e.g.*, ¶[0023], [0027], [0045]; Figs. 1, 2A-B).

In embodiments represented by independent claim 36, a method of controlling a process of fabricating integrated devices on a substrate includes: executing a multi-pass process, wherein the substrate is processed more than once by at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch process is a pass (*see*, *e.g.*, ¶[0023], [0027], [0045]; Figs. 1, 2A-B); measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate, during each at least one measurement process (*see*, *e.g.*, ¶[0023], [0035]; Figs. 1, 2A-B (step 204, 211)); and adjusting a process recipe of the etch process for etching the substrate and a process recipe of at least one pre-etch process and/or at least one post etch process using the results of measuring the dimensions on the structures (*see*, *e.g.*, ¶[0036]-[0037]; Fig. 2A-B (step 206, 207)).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3-18, and 36-53 stand rejected under 35 USC §103 as being unpatentable over US Patent No. 6,625,497, issued September 23, 2003, to *Fairbairn, et al.* (hereinafter *Fairbairn*) in view of US Patent Application Publication No. 2004/0078108, published April 22, 2004, to *Choo, et al.* (hereinafter *Choo*) and further in view of US Patent 6,567,717, issued May 20, 2003, to *Krivokapic, et al.* (hereinafter *Krivokapic*) and US Patent Application No. 2004/0087041 published May 6, 2004 to *Perry, et al.* (hereinafter *Perry*).

2. Claims 19-21 stand rejected under 35 U.S.C. §103 as being unpatentable over *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry*, as applied above to claim 1, and further in view of US Patent Application No. 2003/0022510 published January 30, 2003 to *Morgenstern* (hereinafter *Morgenstern*).

ARGUMENT

Response to Examiner's Answer

The following discussion is in response to the assertions made in the Response to Argument section of the Examiner's Answer (Examiner's Answer, pp. 18-20).

1. 35 USC §103 Claims 1, 3-18, and 36-53

In the Response to Argument's section of the Examiner's Answer, the Examiner asserts that *Fairbairn* discloses 'post-etch processing, such as ash stripping, wet cleaning and/or further CD measurement, by the module before the wafer is returned to the cassette (*Fairbairn, Abstract; Examiner's Answer*, p. 18, ll. 14-16.) The Examiner further asserts that 'the DC [*sic*] measurement, etch processing, and post-etch cleaning are performed at a single module in a controlled environment. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust at least one post-etch process such as cleaning and/or CD measurement or perform it at least one more time to insure the multi-pass process was successful, which reads on appellant's limitation of adjusting at least one post-etch process while forming the at least one structure.' (*Examiner's Answer*, p. 18, ll. 20-21, p. 19, ll. 1-5.) The Appellant's respectfully disagree with the Examiner's assertions.

Specifically, *Fairbairn* is silent on performing a multi-pass process, or repeating a process step more than once. As stated above, and in the passages of *Fairbairn* cited by the Examiner, *Fairbairn* teaches 'feeding back information gathered…….to upcoming lots' (*Fairbairn*, col. 4, ll. 41-43.) Even if at least one post-etch process can be adjusted as the Examiner asserts, it would not have been obvious for one of skill in the art to perform a multi-pass process because the method of *Fairbairn* clearly teaches feeding information to upcoming lots and not performing a multi-pass process on the same substrate.

In addition, the Examiner's asserted motivation "to insure the multi-pass process was successful" is based on an assumption that a multi-step process is performed to begin with and is not consonant with the teachings of *Fairbairn*, alone or in combination with any of the other cited art, as discussed in more detail below.

As further example of the overreaching of the Examiner's argument, the Examiner further states that it would have been obvious to perform the cleaning and/or CD measurement as taught by *Fairbairn* "at least one more time to insure the multi-pass process was successful." (Examiner's Answer, pp. 17-18.) However, such an argument is circular – the motivation to alter *Fairbairn* to yield a multi-pass process cannot be merely so that you will obtain a multi-pass process.

Krivokapic is cited for the proposition that it teaches that, after a post-etch measurement, wafers may be returned to the etch chamber for further etching, if the wafer is under-etched. However, *Krivokapic* merely teaches and suggests further etching of an under-etched workpiece if, and only if, the desired etch results were not obtained during a first etch, and fails to teach a multi-pass process as recited in the claims. The Examiner quotes *Krivokapic* as stating "non-conforming post-etch wafers may be returned for further etching if underetched" and further asserts that this statement "in effect describes a multi-pass process when the under-etch is performed by design." (Final Office Action, p. 6, ll. 3-7.)

The Appellants respectfully disagree with this assertion and submit that the Examiner appears to be using hindsight reconstruction to assert alleged teachings of *Krivokapic*. Specifically, the complete quote from *Krivokapic* is that "[n]onconforming, post-etch wafers may be thrown away if over-etched, or returned for further etching (re-work) if under-etched." Accordingly, it is clear that *Krivokapic* merely recites that, after measurement, if the wafer is over-etched and unsalvageable, then the wafer may be thrown away, but if the wafer is under-etched and may be saved, then it may be returned for re-work. Such re-work is not a multi-pass process as defined in the present claims. *Krivokapic* is silent with respect to performing a multi-pass process as defined in the claims. Moreover, *Krivokapic* is further silent with respect to under-etching wafers on purpose and then re-etching them, as asserted by the Examiner.

The Examiner responds to this argument by stating that *Krivokapic* discloses an automated production system in which feed forward means for feeding forward wafers to minimize tolerance errors of critical performance parameters in processing semiconductor wafers (Examiner's Answer, p. 19, ll. 8-11, citing *Krivokapic*, col. 3, ll. 50-67; col. 4, ll. 1-20) and that "the feed-forward method which returns under-etched

wafers to the etch chamber to be re-etched… is in effect a 'multi-pass process.'" (*Id.,* citing *Krivopavic*, col. 10, ll. 35-38.)

However, the Appellant submit that the Examiner is merely re-asserting the prior position of the Examiner without addressing the argument presented by the Appellants. Specifically, in the first passage cited by the Examiner, *Krivopavic* teaches an automated production system utilized as a feed forward means for feeding forward errors in gate length or sidewall thickness in a variable tilted channel implant (TCI) process. Using the feed forwarded information, the energy and dosage of ions being implanted by the TCI process are adjusted to compensate for errors in gate length or sidewall thickness. (*Krivokapic*, col. 3, ll. 50-67; col. 4, ll. 1-20) The automated production system of *Krivokapic* describes a feed forward means for a variable TCI process, and fails to describe a multi-pass process as recited in the claims. In the second passage cited, the Examiner again merely make the conclusory statement that the *Krivokapic* teaching that "returns under-etched wafers to the etch chamber to be re-etched is "in effect" a multi-pass process."

However, as the Appellants previously noted, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (*In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006) cited with approval in *KSR Int'l v. Teleflex Inc., 127 S. Ct. 1727, 82 USPQ2d 1385, (2007).*) Thus, it is clear that the Examiner appears to be using hindsight reconstruction to assert alleged teachings of *Krivokapic*, as the manner in which the Examiner interprets *Krivokapic* is not taught or suggested by *Krivokapic* itself and is only merely conclusorily stated by the Examiner.

Krivokapic clearly fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1, or executing a multi-pass process, wherein the substrate is processed more than once by at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch

process is a pass; and measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate, during each at least one measurement process, as recited in claim 36.

In addition, the Examiner states, at the end of the Response to Arguments, that the inventions disclosed in the cited references "involve steps that are *inherently multi-pass processes* to enhance production throughput or yield by utilizing information gathered during in-process inspection of the wafers." (*Examiner's Answer*, p. 20, emphasis added.) However, this statement makes clear that the Examiner is ignoring limitations recited in the claims. While the cited art clearly involves multiple processes and steps, none of the cited art discloses a multi-pass process in the manner explicitly recited in the claims.

The Appellants note that the claims do not merely recite any multi-step process, but specifically recite: executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure (in claim 1), and executing a multi-pass process, wherein the substrate is processed more than once by at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch process is a pass (in claim 36). As such, the Appellants submit that a *prima facie* case of obviousness has not been established as the combination of *Fairbairn*, *Choo*, *Krivokapic*, and *Perry* fails to yield the limitations recited in the claims.

As the Examiner has not commented on the arguments relating to the combination of the above-discussed references with *Choo* and *Perry* (relied upon for the present rejections of the above claims), the Appellants maintain that the position urged in the Appeal Brief with respect to the teachings of these references and their combination with the remaining cited art remains unrebutted and should stand.

Thus, the Appellants submit that independents claim 1 and 36, and claims 3-18 and 37-52, respectively depending therefrom, are patentable over *Fairbairn* in view of *Choo*, and further in view of *Krivokapic* and *Perry*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

2. 35 USC §103 Claims 19-21

Independent claim 1, from which claims 19-21 depend, recites limitations not taught or suggested by any permissible combination of the cited art. The patentability of claim 1 over the combination of *Fairbairn*, *Choo*, *Krivokapic*, and *Perry*, and the response to the arguments in the Examiner's Answer, is discussed above.

In addition, in the Response to Arguments section of the Examiner's Answer, the Examiner contends that *Morgenstern* discloses a process to modify the planarization step and the recess etch step in order to arrive at a process that can be better integrated which involves monitoring the thickness of the polysilicon layer by interference spectrometry. (*Examiner's Answer*, p. 19-20, citing *Morgenstern* ¶ [0009] and ¶ [0025].) The Examiner's contention is beyond the scope of dependent claims 19-21, which discloses a capacitive structure of trench capacitor (claim 19) comprising a polysilicon electrode layer (claim 20), and a process etch recipe (claim 21). Further, the Examiner's contention in view of his prior arguments regarding forming a capacitive trench structure makes the motivation of citing *Morgenstern* unclear.

However, even if *Morgenstern* teaches forming a capacitive trench structure, and/or modifying a planarization step and recess etch step as asserted by the Examiner, *Morgenstern* still fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1.

Hence, *Morgenstern* fails to teach or suggest a modification of *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry* that would yield the limitations recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Appellants submit that claims 19-21 are patentable over *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry* and further in view of *Morgenstern*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1, 3-21, and 36-53 as being unpatentable under 35 U.S.C. §103 are improper. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,

May 12, 2008

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CLAIMS APPENDIX

1. (Previously Presented) A method of controlling a process of fabricating integrated devices on a substrate, comprising:

measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate;

adjusting a process recipe of an etch process for etching the substrate and a process recipe of at least one post-etch process using the results of measuring the dimensions on the structures; and

executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure.

2. (Cancelled)

3. (Previously Presented) The method of claim 1, wherein the measuring step further comprises:

detecting a failure of processing equipment performing at least one pre-etch process and/or the at least one post-etch process.

4. (Original) The method of claim 1, wherein the structures are selected from a group consisting of a blanket layer, a featured layer, a film stack having at least one blanket layer and a film stack having at least one featured layer.

5. (Original) The method of claim 1, wherein the measuring step uses a non-destructive measuring technique.

6. (Original) The method of claim 1, wherein the measuring step uses at least one in-situ measuring tool that is a component of an etch reactor performing the etch process.

7. (Original) The method of claim 6, wherein the measuring step further comprises:

measuring thickness of the structures using the at least one in-situ measuring tool.

8. (Original) The method of claim 1, wherein the measuring step uses at least one ex-situ measuring tool that is external to an etch reactor performing the etch process.

9. (Previously Presented) The method of claim 8, wherein the measuring step further comprises:

measuring topographic dimensions and/or thickness of the structures using the at least one ex-situ measuring tool.

10. (Previously Presented) The method of claim 9, wherein the at least one ex-situ measuring tool and the etch reactor are modules of a processing system.

11. (Previously Presented) The method of claim 1, wherein the measuring step is performed external to a processing system utilized to perform the etch process.

12. (Original) The method of claim 1, wherein the adjusting step further comprises:

adjusting the process recipe of an etch process for etching at least one subsequent substrate.

13. (Previously Presented) The method of claim 53, wherein the at least one pre-etch process is performed before measuring the pre-etch dimensions.

14. (Original) The method of claim 1, wherein the at least one post-etch process is performed after measuring the post-etch dimensions.

15. (Previously Presented) The method of claim 1, wherein the at least one post-etch process is selected from a group consisting of a chemical mechanical polishing

process, a deposition process, an etch process, an oxidation process, an annealing process and a lithographic process

16. (Original) The method of claim 1, wherein the pre-etch measurements are taken in a device coupled to a processing system having a processing chamber in which the etch process is performed.

17. (Previously Presented) The method of claim 1, wherein the pre-etch measurements are taken in a device remote from a processing system having a processing chamber in which the etch process is performed.

18. (Original) The method of claim 1, wherein the step of adjusting further comprises adjusting end point detection parameters.

19. (Original) The method of claim 1 wherein the at least one structure is a capacitive structure of a trench capacitor on a substrate.

20. (Original) The method of claim 19, wherein the capacitive structure comprises a polysilicon electrode layer.

21. (Original) The method of claim 20, wherein the process recipe of the etch process further comprises:

providing HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from 1:15 to 15:1.

22-27. (Withdrawn)

28-35. (Cancelled)

36. (Previously Presented) A method of controlling a process of fabricating integrated devices on a substrate comprising:

executing a multi-pass process, wherein the substrate is processed more than once by at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch process is a pass;

measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate, during each at least one measurement process; and

adjusting a process recipe of the etch process for etching the substrate and a process recipe of at least one pre-etch process and/or at least one post etch process using the results of measuring the dimensions on the structures.

37. (Original) The method of claim 36, wherein the measuring step further comprises:

detecting a failure of processing equipment performing the at least one pre-etch process and/or the at least one post-etch process.

38. (Original) The method of claim 36, wherein the structures are selected from a group consisting of a blanket layer, a featured layer, a film stack having at least one blanket layer and a film stack having at least one featured layer.

39. (Original) The method of claim 36, wherein the measuring step uses a non-destructive measuring technique.

40. (Original) The method of claim 36, wherein the measuring step uses at least one in-situ measuring tool that is a component of an etch reactor performing the etch process.

41. (Original) The method of claim 40, wherein the measuring step further comprises:

measuring thickness of the structures using the at least one in-situ measuring tool.

42. (Original) The method of claim 36, wherein the measuring step uses at least one ex-situ measuring tool that is external to an etch reactor performing the etch process.

43. (Previously Presented) The method of claim 42, wherein the measuring step further comprises:

measuring topographic dimensions and/or thickness of the structures using the at least one ex-situ measuring tool.

44. (Previously Presented) The method of claim 43, wherein the at least one ex-situ measuring tool and the etch reactor are modules of a processing system.

45. (Previously Presented) The method of claim 36, wherein the measuring step is performed external to a processing system utilized to perform the etch process.

46. (Original) The method of claim 36, wherein the adjusting step further comprises:

adjusting the process recipe of an etch process for etching at least one subsequent substrate.

47. (Original) The method of claim 36, wherein the at least one pre-etch process is performed before measuring the pre-etch dimensions.

48. (Original) The method of claim 36, wherein the at least one post-etch process is performed after measuring the post-etch dimensions.

49. (Original) The method of claim 36, wherein the at least one pre-etch process and/or the at least one post-etch process is selected from a group consisting of a

chemical mechanical polishing process, a deposition process, an etch process, an oxidation process, an annealing process and a lithographic process.

50. (Original) The method of claim 36, wherein the pre-etch measurements are taken in a device coupled to a processing system having a processing chamber in which the etch process is performed.

51. (Previously Presented) The method of claim 36, wherein the pre-etch measurements are taken in a device remote from a processing system having a processing chamber in which the etch process is performed.

52. (Original) The method of claim 36, wherein the step of adjusting further comprises adjusting end point detection parameters.

53. (Previously Presented) The method of claim 1, further comprising:

adjusting a process recipe of at least one pre-etch process using the results of measuring the dimensions on the structures.

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS APPENDIX

[NONE]